CMOS PROGRAMMABLE PERIPHERAL INTERFACE

TMP82C255AN-2 / TMP82C265AF-2
TMP82C255AN-10 / TMP82C265AF-10

1. GENERAL DESCRIPTION AND FEATURES

The TMP82C255A/TMP82C265A is a CMOS high speed programmable input/output interface with six 8-bit I/O ports. The function is almost equivalent to TMP82C55A×2. The TMP82C265A has the function that ports state are selectable immediately after reset by hardware either in input state or output state.
The TMP82C255A has not this function.

The TMP82C255A/TMP82C265A is fabricated using Toshiba's CMOS Silicon Gate Technology.

(1) 48 programmable I/O terminals (8 bit × 6 ports)

(2) The ports of TMP82C265A are capable to set to output after reset by hardware.

(3) High Speed Version (TRD = 100ns MAX : TMP82C255AN-10/TMP82C265AF-10)

(4) Low power consumption 3mA. Typ.
10μA. MAX. (@5V stand-by)

(5) Three operation modes (Mode 0, Mode 1, Mode 2)

(6) Bit set/reset capability (PC_{00} to PC_{07}, PC_{10} to PC_{17})

(7) All ports are capable of driving darlington transistors
−2.5mA. Typ. @VEXT = 1.5V, REXT = 1.1kΩ

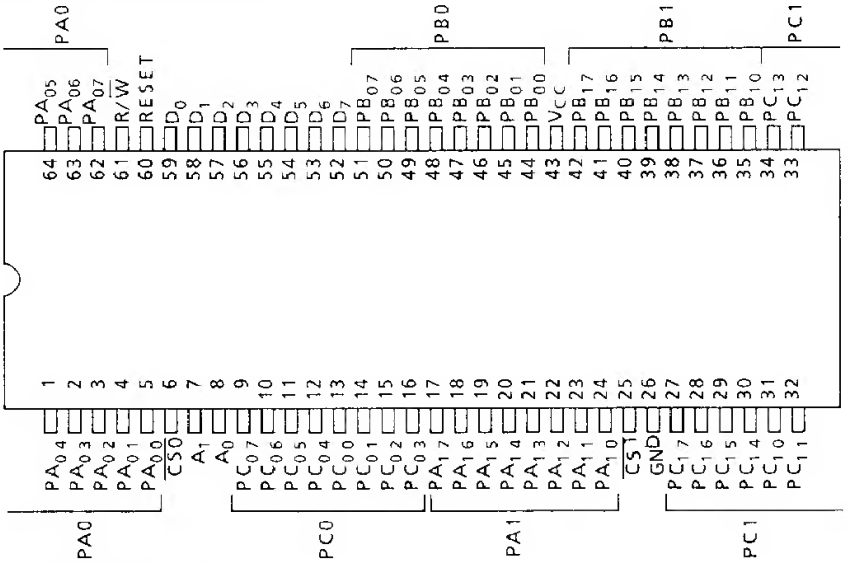
(8) Extended operating temperature : −40°C to +85°C

(9) Two packages

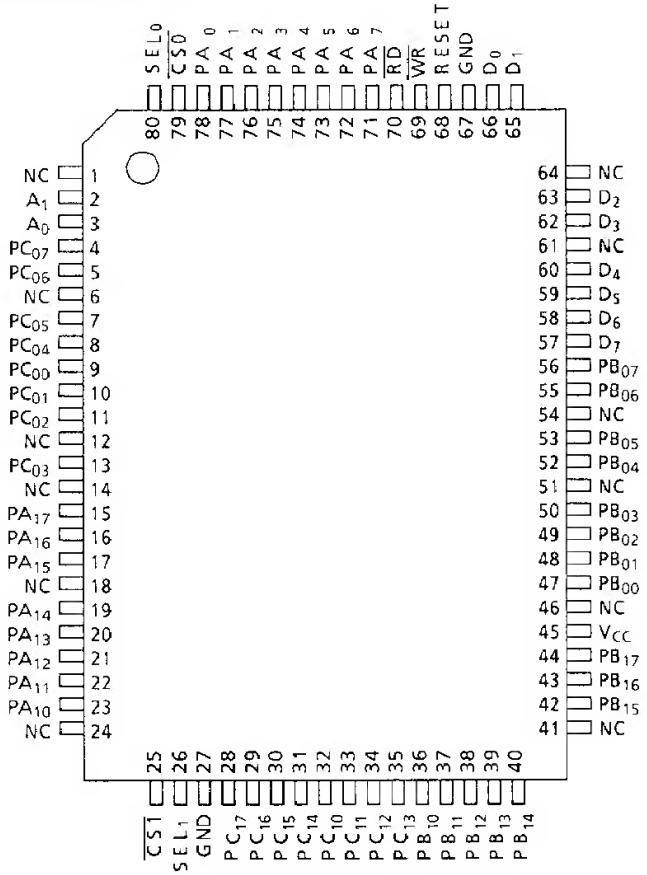
TMP82C255AN	64 PIN Shrink DIP
TMP82C265AF	80 PIN Mini Flat Package

2. PIN CONNECTIONS (TOP VIEW)

TMP82C255AN-2/TMP82C255AN-10



TMP82C265AF-2/TMP82C265AF-10



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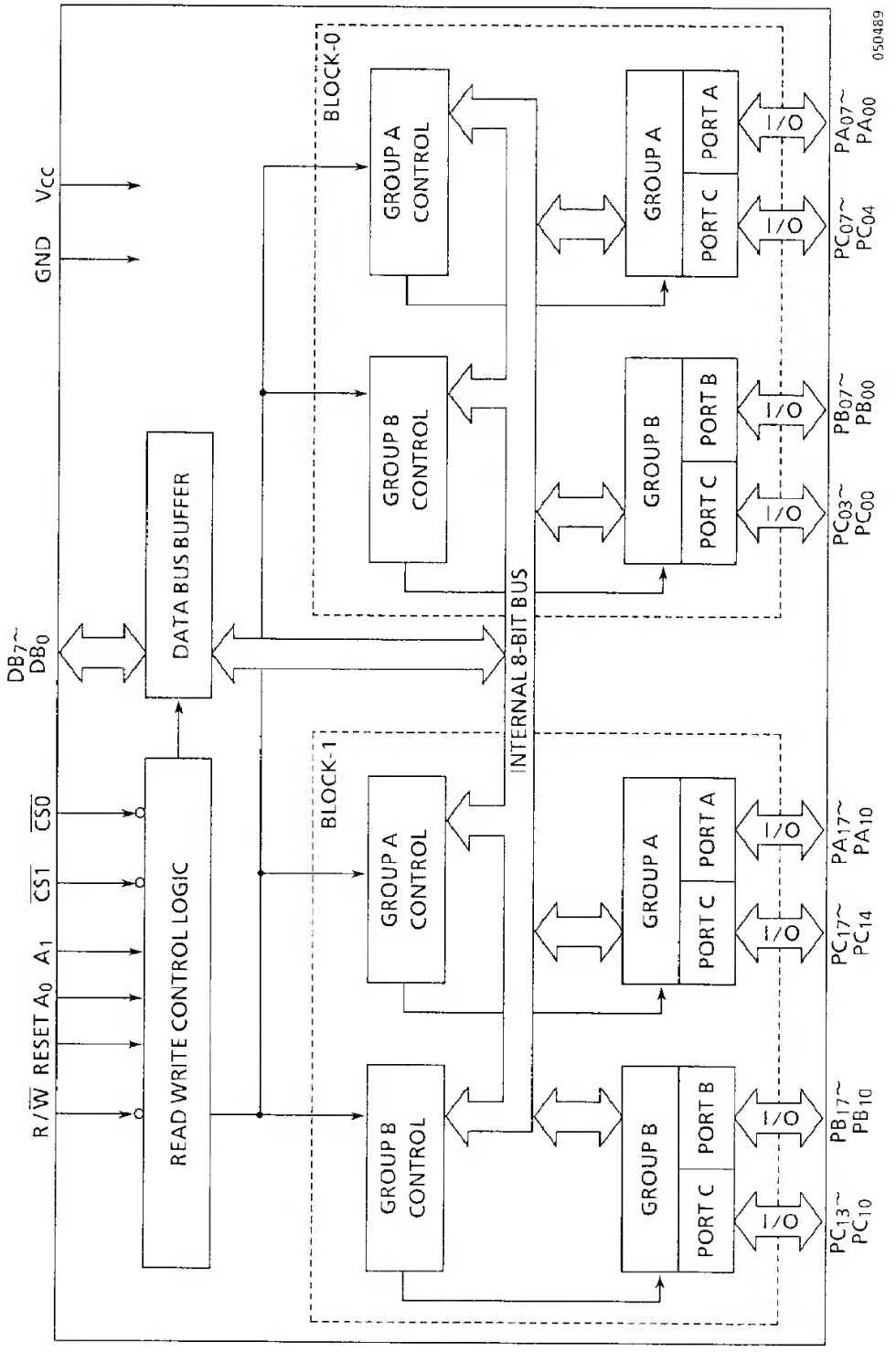
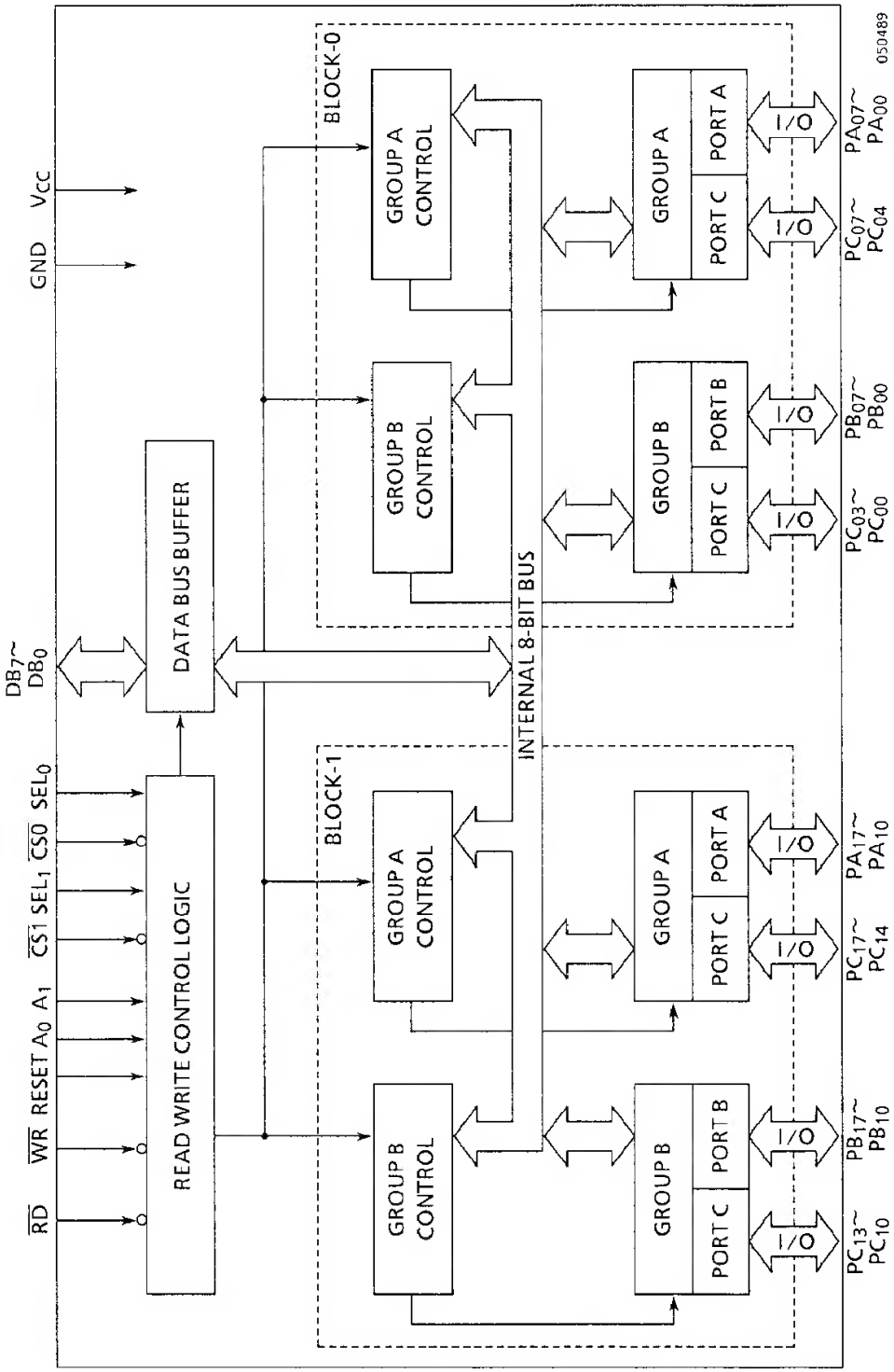
3. BLOCK DIAGRAM

TMP82C255A



TMP82C265A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BLOCK-0
BLOCK-1
GROUP A CONTROL
GROUP B CONTROL
GROUP A
GROUP B
PORT A
PORT B
PORT C
I/O
DATA BUS BUFFER
READ WRITE CONTROL LOGIC
INTERNAL 8-BIT BUS
VCC
GND
DB7~DB0
RD
WR
RESET
A0
A1
CS1
SEL1
CS0
SEL0
PA07~PA00
PC07~PC04
PB07~PB00
PC03~PC00
PA17~PA10
PC17~PC14
PB17~PB10
PC13~PC10

4. PIN NAMES AND PIN FUNCTIONS

Pin Name	Number of Pin	Input/Output 3-state	Function
D_7~D_0	8	I/O 3-state	3-state bidirectional 8-bit data bus. Used for data transfer with MPU. Also, used for transfer of control words to this device and status information from this device.
PA_{07}~PA_{00}	8	I/O 3-state	There are two 3-state 8-bit I/O Port named PA0 and PA1. Operation mode and input/output configuration are defined by software. Port A contains the output latch buffer and input latch.
PA_{17}~PA_{10}	8		
PB_{07}~PB_{00}	8	I/O 3-state	There are two 3-state 8-bit I/O Port named PB0 and PB1. Operation mode and input/output configuration are defined by software. Port A contains the output latch buffer and input latch.
PB_{17}~PB_{10}	8		
PC_{07}~PC_{00}	8	I/O 3-state	There are two 3-state 8-bit I/O Port named PC0 and PC1. Operation mode and input/output configuration are defined by software. Port C can be divided into two 4-bit ports by the mode control and also, used as the control signal for Port A and Port B. In this case, each 3 bits of PC_{00} to PC_{02} and PC_{10} to PC_{12} are used for Port B control and each 5 bits of PC_{03} to PC_{07} and PC_{13} to PC_{17} for Port A control.
PC_{17}~PC_{10}	8		
$\overline{CS0}$	1	Input	Chip select input. When the terminal $\overline{CS0}$ is at "L" level, data transfer between BLOCK-0 and MPU is possible. And when the terminal $\overline{CS1}$ is at "L" level, data transfer between BLOCK-1 and MPU is possible. At "H" level, the data bus is placed in the high impedance state and control from the processor is ignored.
$\overline{CS1}$	1		
A_0, A_1	2	Input	Used for selecting Port A, B, C and the control registers. Normally, this terminal is connected to low order 2 bits of the address bus.
$\overline{RD}$	1	Input	Read signal. Only the TMP82C265A has this terminal. When this terminal is at "L" level, data or status information in this device is transferred to MPU.
$\overline{WR}$	1	Input	Write signal. Only the TMP82C265A has this terminal. When this terminal is at "L" level, data or control word is written into this device from MPU.
R/$\overline{W}$	1	Input	READ/WRITE signal. Only TMP82C255A has this terminal. When the terminal $\overline{CS0}$ or $\overline{CS1}$ is at "L" level, if this terminal is at "H" level, data or status information in this device is transferred to MPU. If this terminal is at "L" level, data or control word is written into this device from MPU.
SEL_0	1	Input	Only the TMP82C265A has these terminals. When SEL_0 or SEL_1 is a "H" level, the ports are set to input state after reset, when it is a "L" level, the ports are set to output state after reset. If the terminals is at "L" level, the function is only capable to set to output state in mode 0. BLOCK-0 ports of block diagram is controled by SEL_0. BLOCK-1 ports of block diagram is controled by SEL_1.
SEL_1	1		
RESET	1	Input	When this terminal is at "H" level, all internal registeres including the control register are cleared, and the function turn out input state in mode 0 for the TMP82C55A and TMP82C265A with SEL_0 or SEL_1 "H" level. THe function turn out output state in mode 0 for the TMP82C265A with SEL_0 or SEL_1 "L" level. Each BLOCK of TMP82C265A is capable to set to different mode by SEL_0 and SEL_1.

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Pin Name	Number of Pin	Input/Output 3-state	Function
V_{CC}	1	Power supply	5V
V_{SS}	1	Power supply	GND

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5. DESCRIPTION OF BASIC OPERATION

5.1 TMP82C255A FUNCTIONS AND FEATURES

The TMP82C255A is a programmable peripheral interface consisting of Block-0 and Block-1 each of which has 3 sets, total 6 sets of 8-bit ports (PA0, PB0, PC0, PA1, PB1 and PC1) each of which has 2 built-in control registers.

Block-0 and Block-1 have the independent chip select input terminals $\overline{CS0}$ and $\overline{CS1}$, respectivery. Data buses D_7-D_0, address input terminals A_1 and A_0, RESET input terminals, and R/$\overline{W}$ terminal are commonly used by Block-0 and Block-1.

Read and Write functions are controlled by one R/$\overline{W}$ terminal and therefore, $\overline{RD}$ and $\overline{WR}$ signals and address must be synthesized and connected to the R/$\overline{W}$, $\overline{CS0}$ and $\overline{CS1}$ terminals.

Total 24 ports input/output terminals each of Block-0 and Block-1 are divided into 12-bit group A and Group B. Group A consist of upper 4 bits of Ports A and Port C, while Group B consists of lower 4 bits of Port B and Port C. Each group is programmable independently by control word from MPU. Three operation modes are available; Mode 0, Mode 1 and Mode 2. In mode 0, it is programmable to use 28-bit input/output ports as the input or output port independently. In Mode 1, the input/output ports are divided into group A and Group B. In each group, 8 bits are used for the input or output port and the remaining 4 bits are used as the control signal. Mode 2 is applicable only to Group A and 12 bits are used for 8-bit two-way bus and 5-bit control signal. Further, when port C is used as the output port, any bit of port C can be set/reset. There are two control registers; one is used for mode setting and the other is used for bit seting/resetting. The control register cannot be read. Further, when the reset input becomes "H" level, the input/output internal registers are all reset and all the input/output terminals are placed in Mode 0 and input Mode (high impedance state).

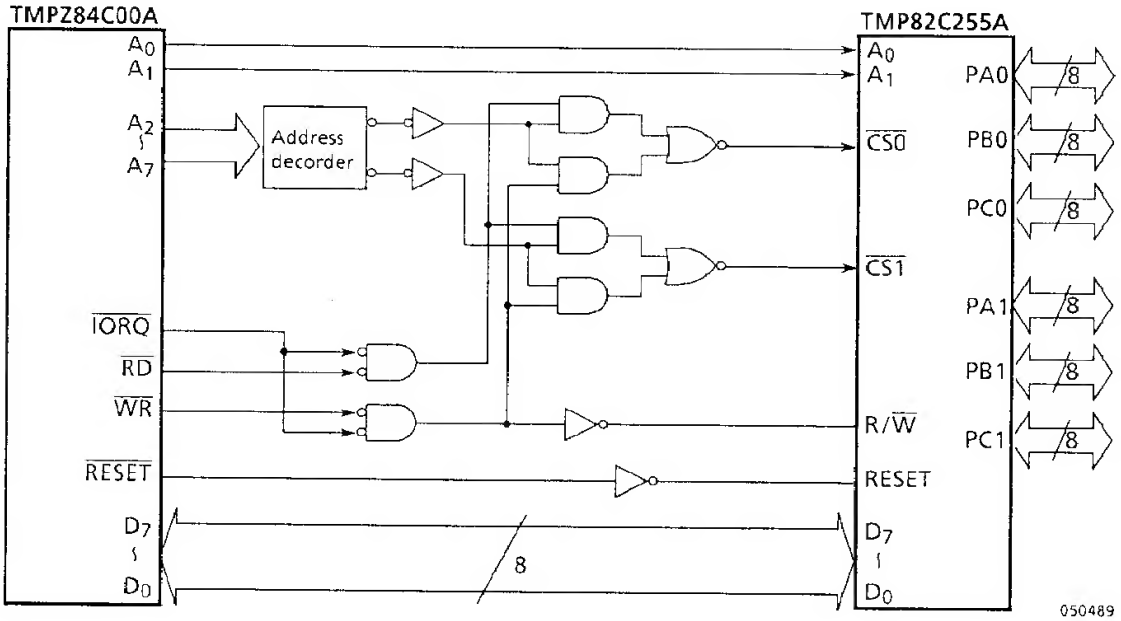

Figure 5.1 Connecting example of TMPZ84C00A and TMP82C255A

In case of the TMP82C255, the read operation is controlled by the terminals $\overline{CS0}$ or $\overline{CS1}$ when the R/$\overline{W}$ terminals is at "H" level and therefore, there is no AC electrical characteristics for rise and fall of the $\overline{RD}$ terminal but anf fall of the $\overline{CS0}$ or $\overline{CS1}$ terminal are controlled.

The write opertion is controlled by the terminal $\overline{CS0}$ or $\overline{CS1}$ when the R/$\overline{W}$ is at "L" level. Further, the maximum control of the setup time TWC of the $\overline{CS0}$ or $\overline{CS1}$ for fall of R/$\overline{W}$ terminal and the hold time T_{WC} of the $\overline{CS0}$ or $\overline{CS1}$ for the rise of R/$\overline{W}$ terminal is added. This is because the $\overline{CS0}$ or $\overline{CS1}$ terminal controls the read operation when the R/$\overline{W}$ is at "H" level.

5.2 TMP82C255A BASIC OPERATION

Basic operation of the TMP82C255A for BLOCK-0. PC0 are as shown in Table 5.1.

Table 5.1 Basic Operation for Block-0 of the TMP82C255A

$\overline{CS0}$	RESET	A_1	A_0	R/$\overline{W}$	Function
×	1	×	×	×	Set to all ports (six ports) input state in mode 0. Ports terminals are in High Impedance state.
0	0	0	0	1	Data Bus ← PA0
0	0	0	1	1	Data Bus ← PB0
0	0	1	0	1	Data Bus ← PC0
0	0	0	0	0	PA_0 ← Data Bus
0	0	0	1	0	PB_0 ← Data Bus
0	0	1	0	0	PC_0 ← Data Bus
0	0	1	1	0	Control register for BLOCK-0 ← Data Bus
0	0	1	1	1	Inhibition of combination
1	0	×	×	×	Non active

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Basic Operation for BLOCK-1 of the TMP82C255A is equal to the one shown in Table 5.1. BLOCK-1 is selected when $\overline{CS1} = 0$.

5.3 TMP82C265A FUNCTION AND FEATURES

The TMP82C265A can be set to general mode when the terminal SEL_0 or SEL_1 is fixed at "H" level and to the output mode when it is fixed at "L" level.

In the general mode, the TMP82C265A has the functions similar to those of the TMP82C55A but for the $\overline{WR}$ and $\overline{RD}$ functions, the independent $\overline{RD}$ and $\overline{WR}$ terminals are provided as in the former TMP82C255A unlike R/$\overline{W}$ 1 terminal in the TMP82C255A. Therefore, the TMP82C265A operates when connected in the same connecting method as before.

In the output mode, all ports of the TMP82C265A are set in "L" output state in mode 0 after reset. Further, even when the write operation is made in any mode, the ports are set in output state in mode 0, and "L" level signals are output from the ports.

5.4 TMP82C265A BASIC OPERATION

Basic operation of the TMP82C265A in the general mode (the terminal SEL_0-SEL_1 is "L" level) is equal to that of the TMP82C255A.

Basic operation for BLOCK-0 of the TMP82C265A in the output only mode (SEL_0: "L" level) is as shown in Table 5.2.

Table 5.2 Output Mode Basic Operation for Block-0 of the TMP82C265A

SEL_0	$\overline{CS0}$	RESET	D_7	A_1	A_0	$\overline{RD}$	$\overline{WR}$	Function
0	×	1	×	×	×	×	×	Set to PA0, PB0 and PC0 ports "L" level output state in mode 0
0	0	0	1	1	1	1	0	PA0, PB0 and PC0 ports "L" level output state in mode 0 set command
×	0	0	0	1	1	1	0	Bit set/reset control
△	0	0	×	0	0	1	0	PA0 ← Data Bus
△	0	0	×	0	1	1	0	PB0 ← Data Bus
△	0	0	×	1	0	1	0	PC0 ← Data Bus
△	0	0	×	0	0	0	1	Data Bus ← PA0 (Read the terminal state)
△	0	0	×	0	1	0	1	Data Bus ← PB0 (Read internal output latch)
△	0	0	×	1	0	0	1	Data Bus ← PC0 (Read internal output latch)

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△ : The output only mode is maintained when SEL_0 is either in "L" or "H" level if set to the output state.
However, if the RESET terminal is set to "H" level or mode is written when SEL_0 is at "H" level, the output mode is changed to the general mode.

Basic operation of the TMP82C265A for Block-1 is equal to that shown in Table 5.2 but the control is made by the terminal SEL_1 and $\overline{CS1}$.

6. DETAILED OPERATIONAL DESCRIPTION

The operation of the TMP82C255A and TMP82C265A in the general made is described in detail. Further, the operation is described for Block-0. Block-1 has the same functions as those of Block-0 and therefore, it is omitted.

The operation of the TMP82C265A in the output mode is considered to be a special case of the description for the general mode provided below, in which the TMP82C265A has been set in the output state in mode 0 from immediately after reset irrespective of command input and therefore, the description is omitted here.

6.1 MODE SELECTION

There are three basic modes of operation that can be selected by control words.

Mode 0 - Basic I/O (Group A, Group B)

Mode 1 - Strobe input/Strobe output(Group A, Group B)

Mode 2 - Two-way bus(Port A only)

Operation modes for Group A and Group B can be independently defined by the control word from the MPU. If D_7 is set to "1" in writing a control word into the PPI, on operation mode is selected, while of D_7 = "0" , the set/reset function for Port C is selected.

6.1.1 Control Word to Define Operation Mode

Figure 6.1 shows the control words to define operation mode of the TMP82C255A/TMP82C265A.

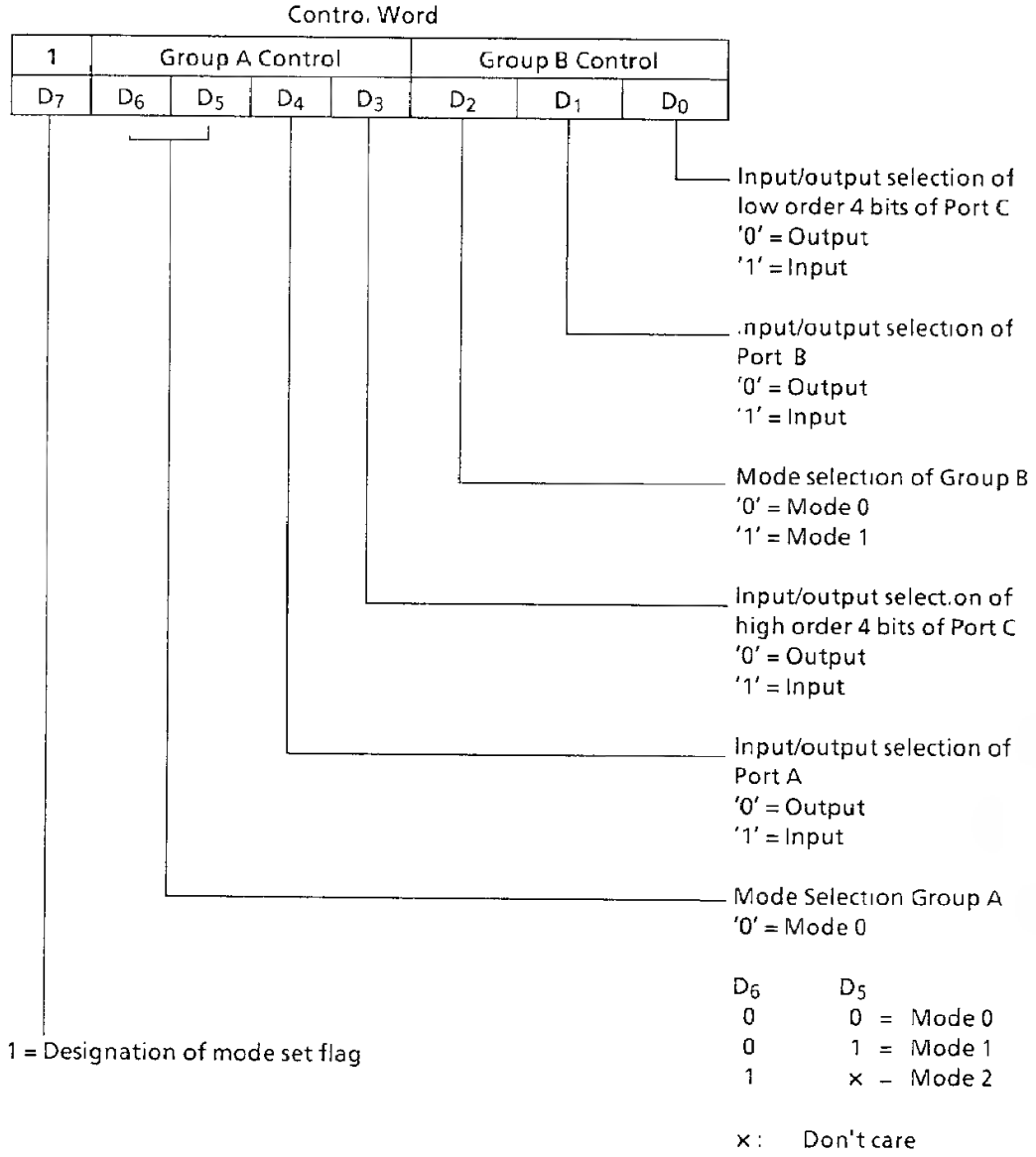

Figure 6.1 Control Word for Mode Selection

6.1.2 Port C Bit Set/Reset Control Word

Any bit of 8 bits of Port C can be set/reset by Port C bit set/reset control word. Figure 6.2 shows the Port C bit set/reset control word.

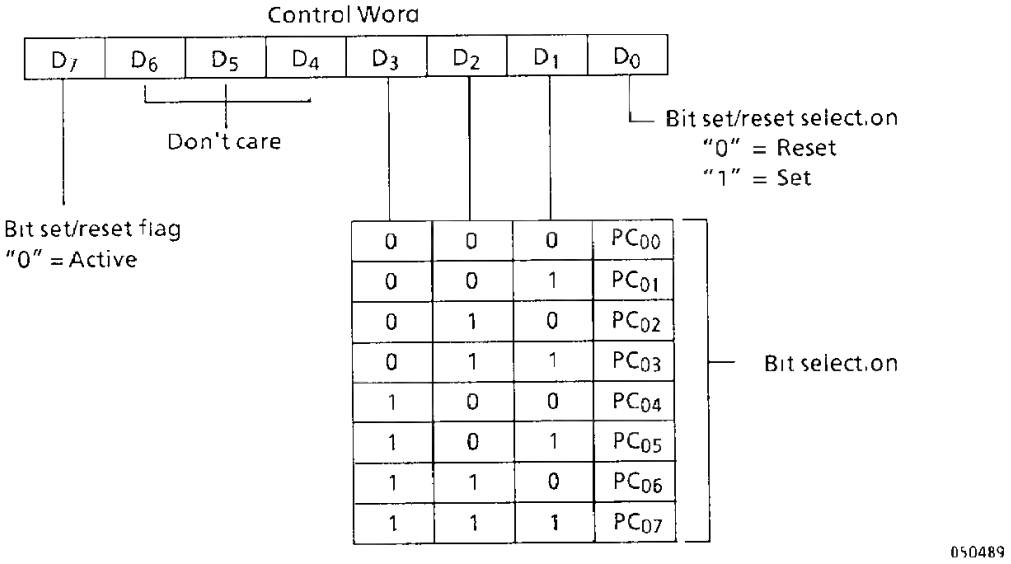

Figure 6.2 Control Word for Bit Set/Reset

6.2 OPERATION MODES

6.2.1 Mode 0 (Basic I/O)

This functional configuration is used for simple input or output operations. No 'handshaking' is required and data is simply written to or read from a specified part. Output data to the ports from MPU are latched out but input data from the ports are not latched.

In Mode 0, 24 I/O terminals are divided into four groups of Port A (8 bits) , Port B (8 bits) , high order 4 bits of Port C and low order 4 bits of Port C. Each port can be programmed to be input or output. The configuration of each port are determined according to the contents of Bit 4 (D_4) , 3 (D_3) , 1 (D_1) and 0 (D_0) of the control word for mode selection.

The I/O configuration of each port in Mode 0 are shown in Table 6.2.

Table 6.2 Port definition in Mode 0

Mode Setting Control Word				Port A	Port C (PC_{07}~PC_{04})	Port B	Port C (PC_{03}~PC_{00})
D_4	D_3	D_1	D_0				
0	0	0	0	Out	Out	Out	Out
0	0	0	1	Out	Out	Out	In
0	0	1	0	Out	Out	In	Out
0	0	1	1	Out	Out	In	In
0	1	0	0	Out	In	Out	Out
0	1	0	1	Out	In	Out	In
0	1	1	0	Out	In	In	Out
0	1	1	1	Out	In	In	In
1	0	0	0	In	Out	Out	Out
1	0	0	1	In	Out	Out	In
1	0	1	0	In	Out	In	Out
1	0	1	1	In	Out	In	In
1	1	0	0	In	In	Out	Out
1	1	0	1	In	In	Out	In
1	1	1	0	In	In	In	Out
1	1	1	1	In	In	In	In

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6.2.2 Mode 1 (Strobe I/O)

In Mode 1, input/output of port data is performed in conjunction with the srtobe signals or 'handshaking' signals. Port C is used to control Port A or Port B.

The basic operatings in Mode 1 are as follows:

- Mode 1 can be set for two groups of Group A and Group B.
- Each group consist of 8-bit data port and 4-bit control/data port.
- The 8-bit data port can be set as input or output port.
- The control/data port is used as control or status of the 8-bit data port.

(1) When used as the input port in Mode 1 :

- $\overline{STB}$ (Strobe Input)

  At "0", input data is loaded in the internal input latch in the port.
  In this case, a control signal from MPU is not concerned and data is input from the port any time. This data is not read out on the data bus unless MPU executes an input instruction.

- IBF (Input Buffer Full F/F Output)

  When data is loaded in the internal input latch from the port, this output is set to "1". IBF is set ("1") by $\overline{STB}$ input being reset and is reset ("0") by the rising edge of $\overline{RD}$ input.

- INTR (Interrupt Request Output)

  Used for the interrupt process of data loaded in the internal input latch. When $\overline{STB}$ input is at "0" if INTE (INTE flag) in the PPI is in the enabled state ("1"), IBF is set to "1". INTR is set to "1" immediately after the rising edge of this $\overline{STB}$ input and reset to "0" by the falling edge of $\overline{RD}$ input.

  The INTE flags of Group A and Group B are controlled as follows:

  INTEA – Control by bit set/reset of PC_{04}

  INTEB – Control by bit set/reset of PC_{02}

(2) When used as the output port in Mode 1:

- $\overline{OBF}$ (Output Buffer Full F/F Output)

  This is a flag which shows that MPU has written data into a specified port. $\overline{OBF}$ is set to becomes "0" at the rising edge of $\overline{WR}$ signal and is set to "1" at the falling edge of $\overline{ACK}$ (Acknowledge input) signal.

- $\overline{ACK}$ (Acknowledge Input)

  $\overline{ACK}$ signal is sent to the PPI as a response from a peripheral device that received data from the port.

- INTR (Interrupt Request Output)

  When a peripheral device received data from MPU, INTR is set to "1" and the interrupt is requested to MPU. If ACK signal is received when INTE flag is in the enable state, $\overline{OBF}$ is set to "1" and INTR signal becomes "1" immediately after the rising edge of $\overline{ACK}$ signal. Further, INTR is reset at the falling edge of $\overline{WR}$ signal when data is written into the PPI by MPU.

  The INTE flags of Group A and Group B are controlled as follows:

  INTEA – Control by bit set/reset of PC_{06}

  INTEB – Control by bit set/reset of PC_{02}

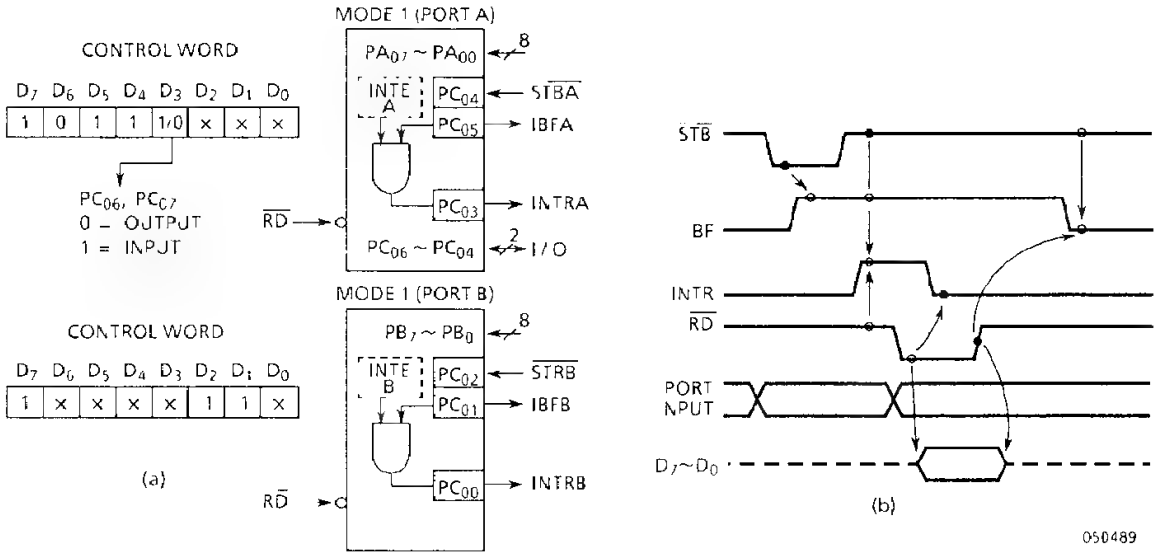

Figure 6.3 Example of Strobe Input in Mode 1

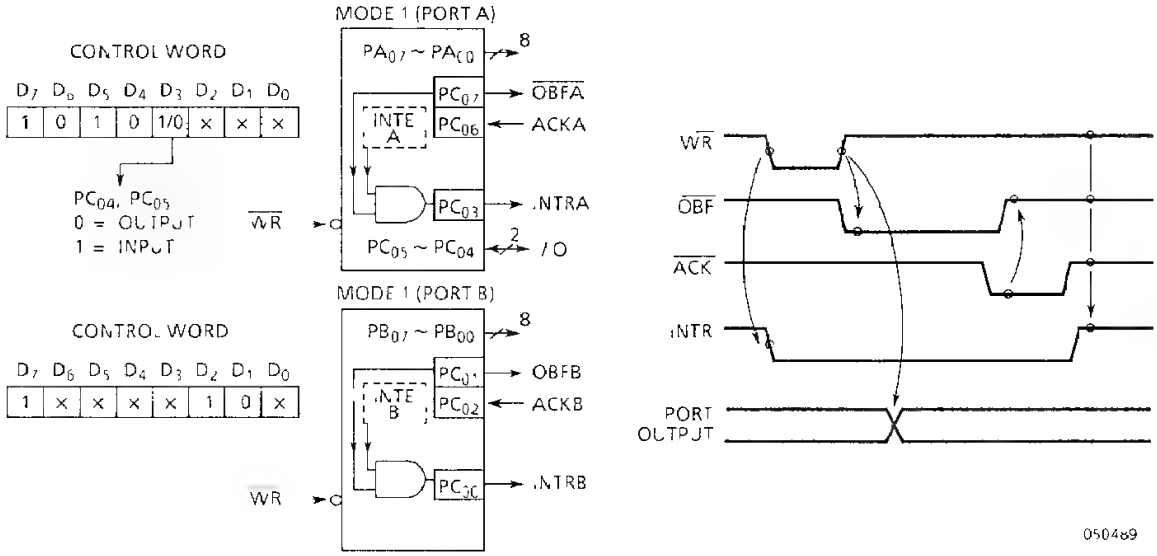

Figure 6.4 Example of Strobe Output in Mode 1

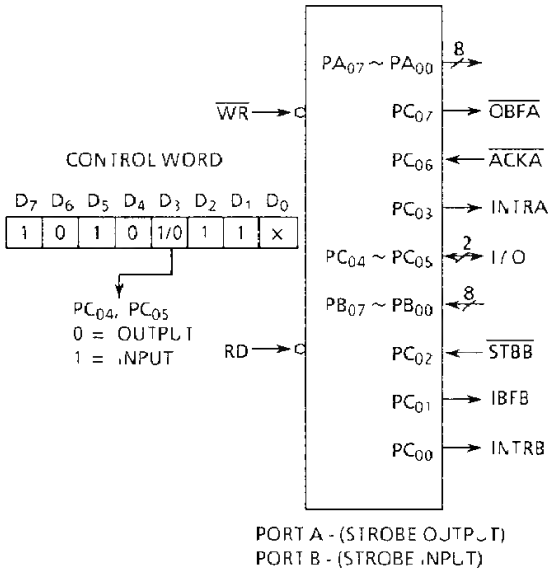

Figure 6.5 Example of Port A Output, port B Input in Mode 1

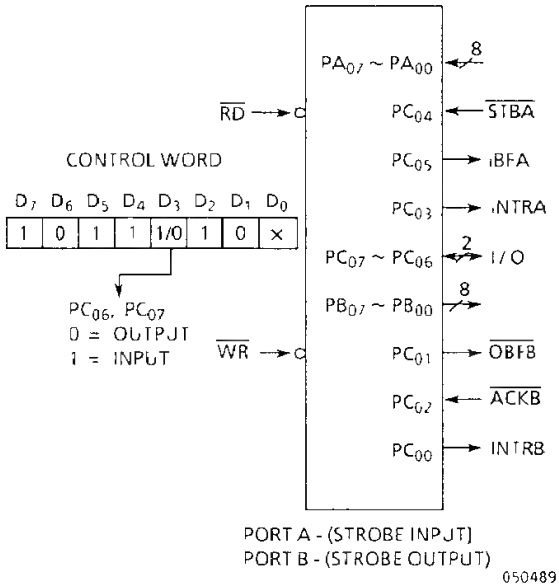

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Figure 6.6 Example of Port A Input, Port B Output in Mode 1

6.2.3 Mode 2 (Strobed Bidirectional Bus I/O)

In this mode, Port A is used as 8 bits bidirectional bus for data transfer with a peripheral device. This mode is applicable only to Group A, which consists of an 8-bit bidirectional bus (Port A 8-bit) and 5-bit control signals (high order 5 bits of Port C). The bidirectional bus (Port A) has both the internal input and output registers. When group A is set in Mode 2, Group B can be set independently. There are 5 control signals as follows when Group A is used in Mode 2.

- OBF (Output buffer Full F/F Output)

  When MPU writes data into of Port A, $\overline{OBF}$ is set to "0" to inform a peripheral device that the PPI is ready to output data. However, Port A is kept in the floating (high impedance) state until $\overline{ACK}$ input signal is received.

- $\overline{ACK}$ (Acknowledge Input)

  When $\overline{ACK}$ signal is set to "0", the data of the 3-state output buffer of Port A is send out. If $\overline{ACK}$ signal is at "1", Port A is in the high impedance state.

- $\overline{STB}$ (Strobe Input)

  When $\overline{STB}$ input is set to "0", the data from peripheral devices are held in the input latch. When the active RD signal is input into the PPI, the latched input data are output on the system data bus (D_7-D_0).

- IBF (Input Buffer Full F/F Output)

  When data from peripheral devices are held in the input latch, IBF is set to "1".

- INTR (Interrupt Request Output)

  INTR is the output to request the interrupt to MPU and its function is the same as that in Mode 1. There are two interrupt enable flip-flop (INTE), INTE1 corresponds to INTEA in Mode 1 output and INTE2 to INTEA in Mode 1 input.

  INTE 1 – Used to generate INTR signal in conjunction with $\overline{OBF}$ and $\overline{ACK}$ signals, and is controlled by PC_{06} bit set/reset.

  INTE2 – Used to generate INTR signal in conjunction with IBF and $\overline{STB}$ singals, and is coutrolled by PC_{04} bit set/reset.

Figure 6.7 shows the operating example and the timing diagram in Mode 2.

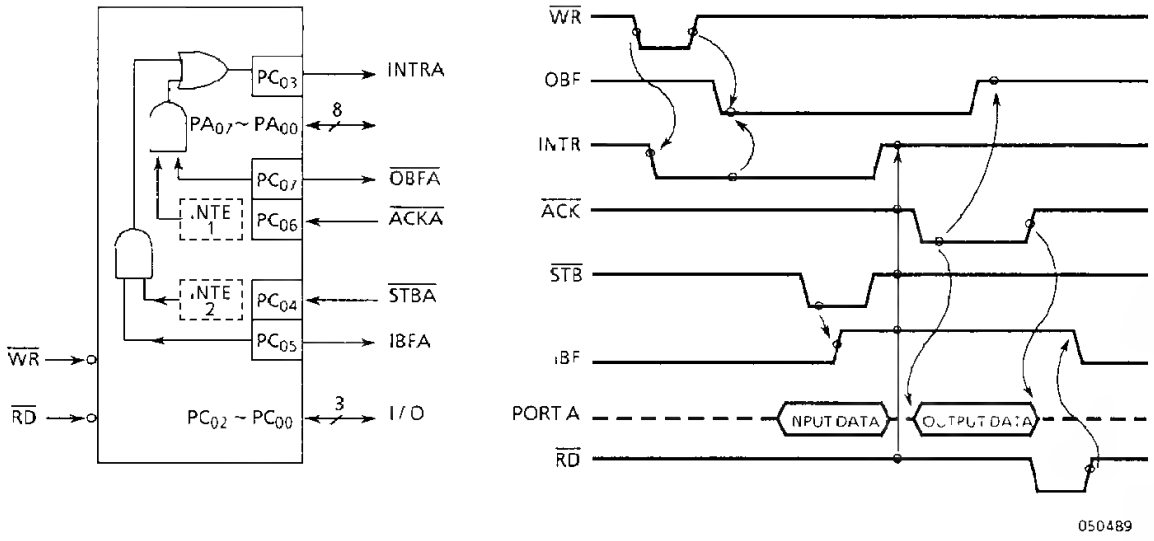

Figure 6.7 Oerating example in Mode 2

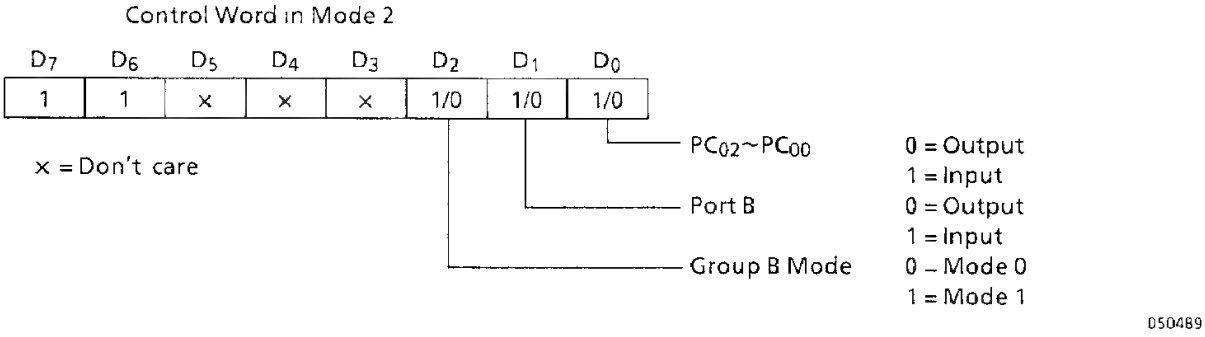

Figure 6.8 Control Word and Configuration in Mode 2

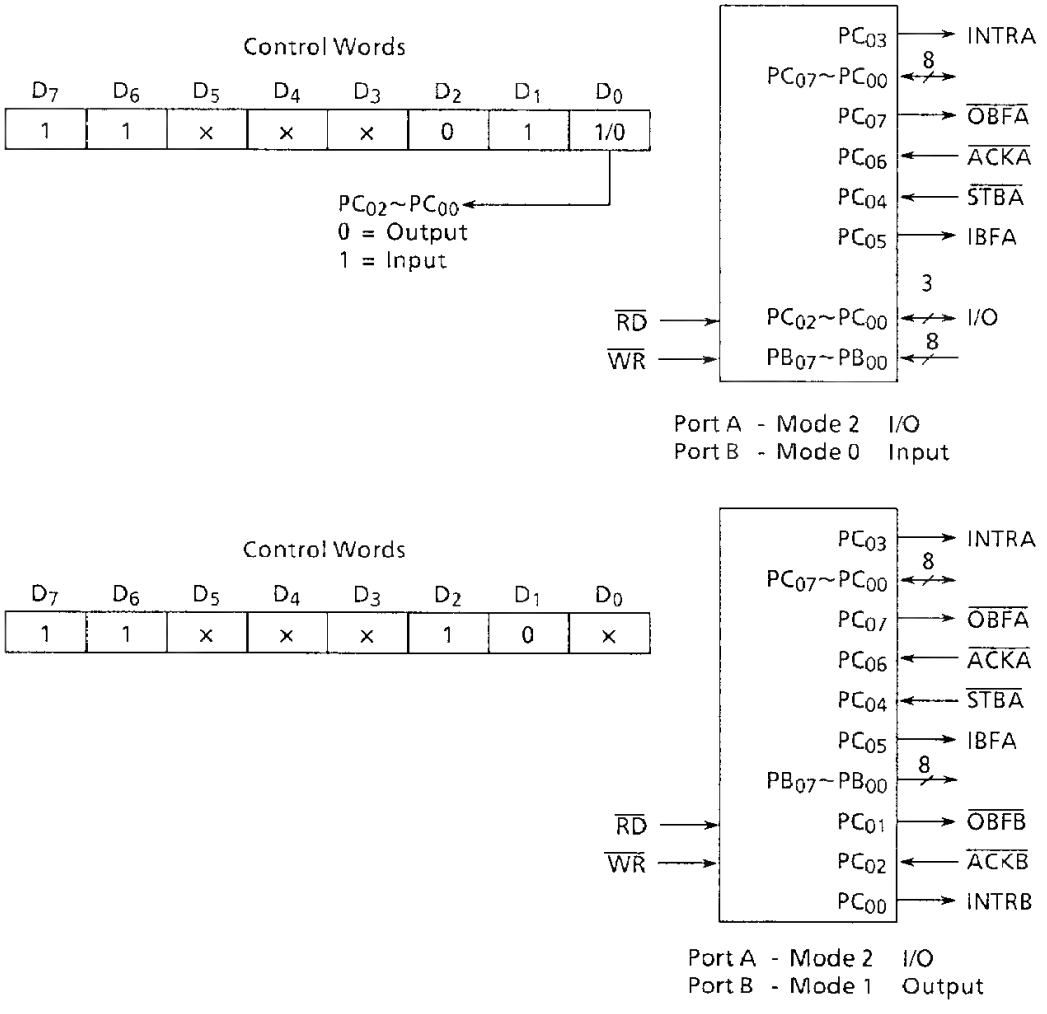

Figure 6.9 Example in Combination with Mode 2 and Other Mode

6.2.4 Precautions for use in Mode 1 and 2

When used in Mode 1 and 2, bits which are not used as control or status in Port C can be used as follow.

If porgrammed as the input, they are accessed by normal Port C read.

If porgrammed as the output, high order bits of Port C (PC_{07}-PC_{04}) are accessed using the bit set/reset function. As to low order bits of Port C (PC_{03}-PC_{00}), in additions to access by the bit set/reset function, 3 bits only can be accessed by normal writing.

6.3 READING PORT C STATUS

When Port C is used as the control port, that is, when Port C is used in Mode 1 or Mode 2, the status information of the control word can be read out by a normal read operation of Port C.

Table 6.3 Status Word Format of Port C

Data Mode	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1 Input	I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
Mode 1 Output	$\overline{OBFA}$	INTEA	I/O	I/O	INTRA	INTEB	$\overline{OBFB}$	INTRB
Mode 2	$\overline{OBFA}$	INTE1	IBFA	NTE2	INTRA	By Group B Mode		

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7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Symbo	Item	Rating	Unit
V_{CC}	Supply Voltage	− 0.5~7.0	V
V_{IN}	Input Voltage	− 0.5~V_{CC} + 0.5	V
P_D	Power Dissipation	250	mW
T_{SOLDER}	So dring Temperature (10sec)	260	°C
T_{STG}	Storage Temperature	− 65~ + 150	°C
T_{OPR}	Operating Temperature	− 40~ + 85	°C

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7.2 DC ELECTRICAL CHARACTERISTICS

TA = − 40°C to + 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

Symbol	tem	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		− 0.5	−	0.8	V
V_{IH}	Input H gh Voltage		2.2	−	V_{CC} + 0.5	V
V_{OL}	Output Low Vo tage	I_{OL} = 2.5mA	−	−	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = − 400μA	2.4	−	−	V
V_{OH2}	Output High Voltage	I_{OH} = − 100μA	V_{CC} − 0.8	−	−	V
I_L	.nput Leak Current	0 ≤ V_{IN} ≤ V_{CC}	−	−	± 10	μA
I_{OL}	Output LeaK Current (High Impedance State)	0 ≤ V_{OUT} ≤ V_{CC}	−	−	± 10	μA
I_{DAR}	Darlington Drive Current	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ	− 1.0	−	-5 0	mA
I_{CC1}	Operating Supply Current	I / O cycle Time 1μsec		3.0	5.0	mA
I_{CC2}	Stand-by Supply Current	V_{IH} > V_{CC}-0.2V V_{IL} < 0.2V CS > V_{CC} − 0.2V	−	−	10	μA

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* Total current of all darlington drive ports must not exceed 60mA.

7.3 CAPACITANCE

$T_A = 25°C$, $V_{CC} = V_{SS} = 0V$

Symbol	Item	Test Condition	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	f = 1MHz (*)	—	-	10	pF
$C_{I/O}$	I/O Capacitance		—	—	20	pF

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(*): All terminals except that to be measured should be earthed.

7.4 AC ELECTRICAL CHARACTERISTICS (1/2)

$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	A - 2		A - 10		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address set-up time for $\overline{RD}$ fall	0	—	0	—	ns
t_{RA}	Address hold time for $\overline{RD}$ rise	0	—	0	—	ns
t_{RR}	$\overline{RD}$ pulse width	160	—	150	—	ns
t_{RD}	Delay from $\overline{RD}$ fal to decided data output	—	140		100	ns
t_{DF}	Time from $\overline{RD}$ rise to data bus floating	0	40	0	40	ns
t_{RV}	Time from RD or $\overline{WR}$ rise to next RD or WR fall	200	—	180	—	ns
t_{AW}	Address set-up time for $\overline{WR}$ fall	20	—	20	—	ns
t_{WA}	Address holding time for $\overline{WR}$ rise	0	—	0	—	ns
t_{WW}	$\overline{WR}$ pulse width	120	—	120	—	ns
t_{DW}	Bus data set-up time for $\overline{WR}$ rise	100	—	100	—	ns
t_{WD}	Bus data holding time for $\overline{WR}$ rise	20	—	20		ns
t_{WB}	Delay from $\overline{WR}$ rise to decided data output	—	350	—	350	ns
t_{IR}	Port data set-up time for $\overline{RD}$ fall	0	-	0	—	ns
t_{HR}	Port data holding time for RD rise	0	—	0	—	ns
t_{AK}	$\overline{ACK}$ pulse width	300	—	300	—	ns
t_{ST}	$\overline{STB}$ pulse width	350	—	350	—	ns
t_{PS}	Port data set-up time for $\overline{STB}$ rise	20	—	20	—	ns
t_{PH}	Port data holding time for $\overline{STB}$ rise	150	—	150	—	ns
t_{AD}	Delat from $\overline{ACK}$ fall to decided data output Delay	—	300	—	300	ns
t_{KD}	Time from $\overline{ACK}$ rise up to port (Port in Mode 2) floating	25	250	20	250	ns
t_{WOB}	Delay from $\overline{WR}$ rise to $\overline{OBF}$ fall	—	300	—	300	ns
t_{AOB}	Delay from $\overline{ACK}$ fall to $\overline{OBF}$ rise	—	350	—	350	ns
t_{SIB}	Delay from $\overline{STB}$ fall to IBF rise	—	300		300	ns

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AC ELECTRICAL CHARACTERISTICS (2/2)

Symbol	Parameter	A-2		A-10		Unit
		Min.	Max.	Min.	Max.	
t_{RB}	Delay from $\overline{RD}$ fall to IBF rise	—	300	—	300	ns
t_{RIT}	Delay from $\overline{RD}$ fall to INTR fall	—	400	—	400	ns
t_{ST}	Delay from $\overline{ACK}$ rise to INTR rise	—	300	—	300	ns
t_{AIT}	Delay from $\overline{ACK}$ rise to INTR rise	—	350	—	350	ns
t_{WIT}	Delay from WR rise to INTR fall	—	450	—	450	ns
t_{AC}	Address set-up time for $\overline{CS0}$, $\overline{CS1}$ fall	0	—	0	—	ns
t_{CA}	Address hold time for $\overline{CS0}$, $\overline{CS1}$ rise	0	—	0	—	ns
t_{CC}	$\overline{CS0}$, $\overline{CS1}$ pulse width	160	—	150	—	ns
t_{CD}	Delay from $\overline{CS0}$, $\overline{CS1}$ fall to decided data output	—	140	—	100	ns
t_{DFC}	Time from $\overline{CS0}$, $\overline{CS1}$ rise to data bus floating	0	40	0	40	ns
T_{CW}	CS0, CS1 set-up time for R/$\overline{W}$ fall	—	0	—	0	ns
T_{WC}	$\overline{CS0}$, $\overline{CS1}$ holding time for R/$\overline{W}$ rise	—	50	—	50	ns
t_{IC}	Port data set-up time for $\overline{CS0}$, $\overline{CS1}$ fall	0	—	0	—	ns
t_{HC}	Port data holding time for $\overline{CS0}$, $\overline{CS1}$ rise	0	—	0	—	ns
t_{CIB}	Delay from $\overline{CS0}$, $\overline{CS}$ fall to $\overline{IBF}$ rise	—	300	—	300	ns
t_{CIT}	Dekay from $\overline{CS0}$, $\overline{CS1}$ fall to $\overline{INTR}$ fall Delay	—	400	—	400	ns
t_{RES}	RESET pulse width	500	—	500	—	ns

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Note 1 :

A-2 : TMP82C255AN-2, TMP82C265AF-2

A-10 : TMP82C255AN-10, TMP82C265AF-10

Note 2 :

Following AC specifications of TMP82C255A are applied to the logical AND timing between R/$\overline{W}$ terminal and $\overline{CS0}$ or $\overline{CS1}$ terminal.

Symbol			
T_{AW}	T_{WA}	T_{DW}	T_{WD}
T_{WB}	T_{CW}	T_{WC}	

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Note 3 :

AC Measuring Point Input Voltage $V_{IH}=2.4V$, $V_{IL}=0.45V$

Output Voltage $V_{OH}=2.2V$, $V_{OL}=0.8V$

$CL=150pF$.

8.1 TMP82C255A TIMING DIAGRAM (1)

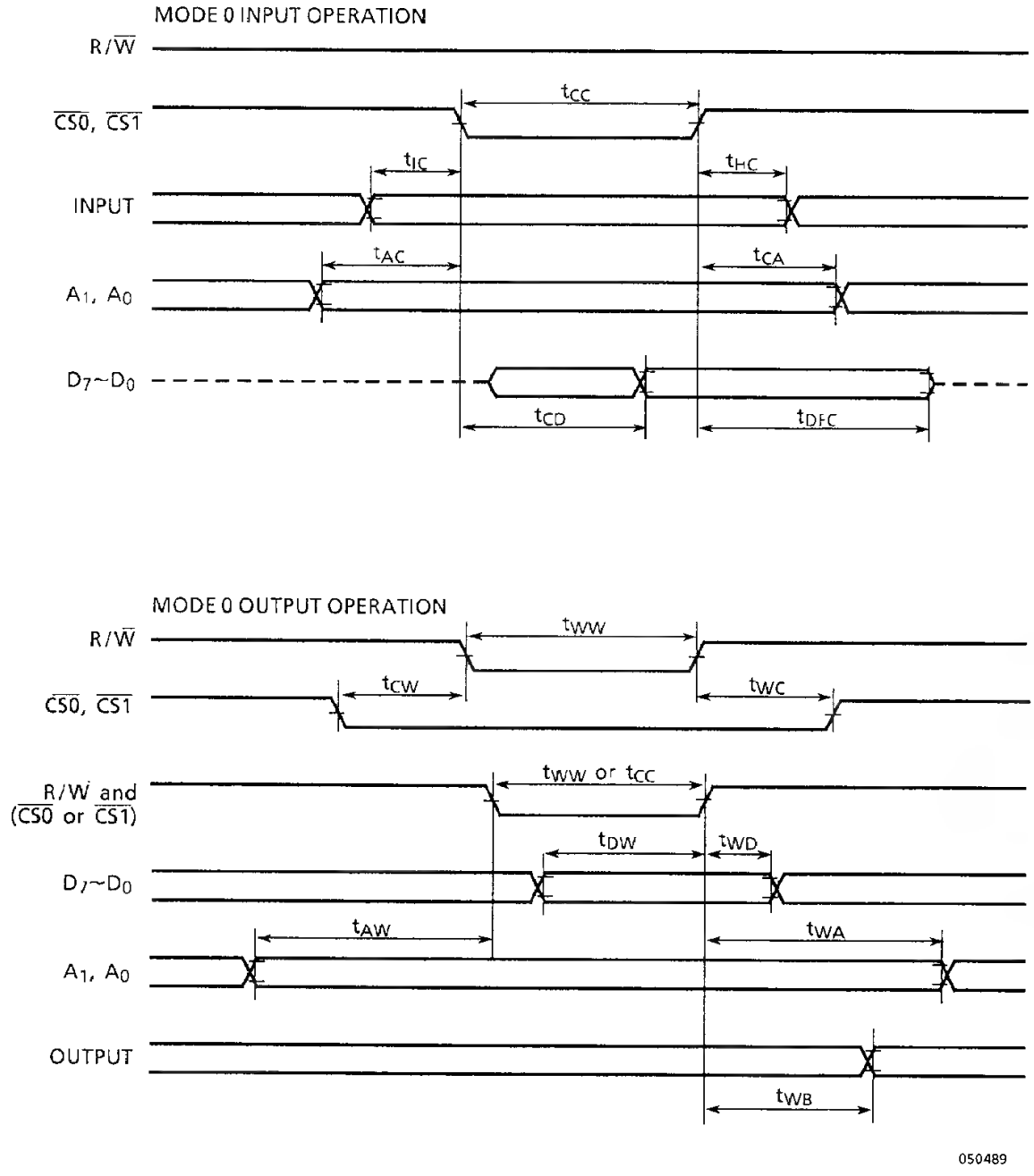


Figure 8.1 TMP82C255A Timing diagram (1)

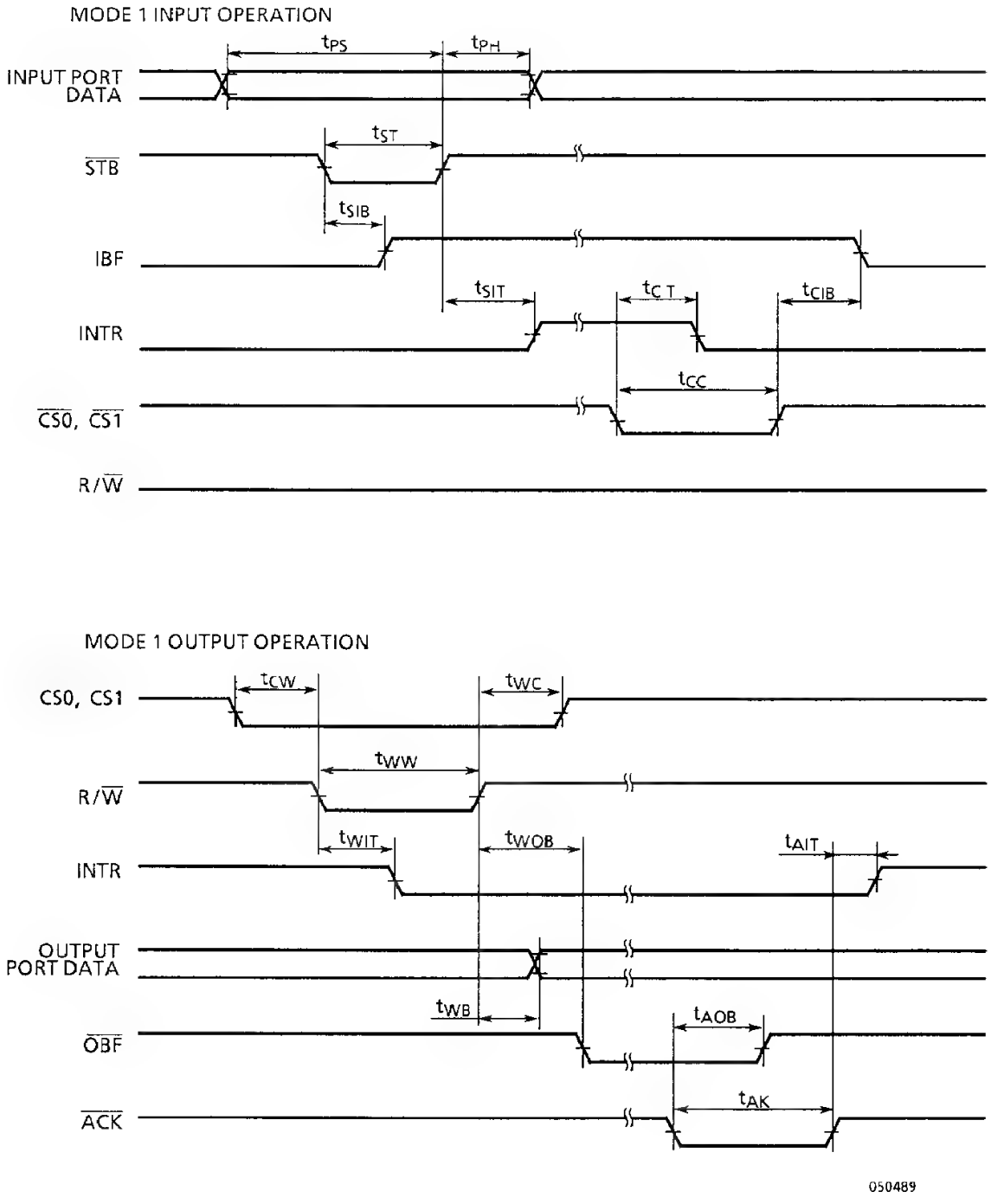


Figure 8.1 TMP82C255A Timing diagram (2)

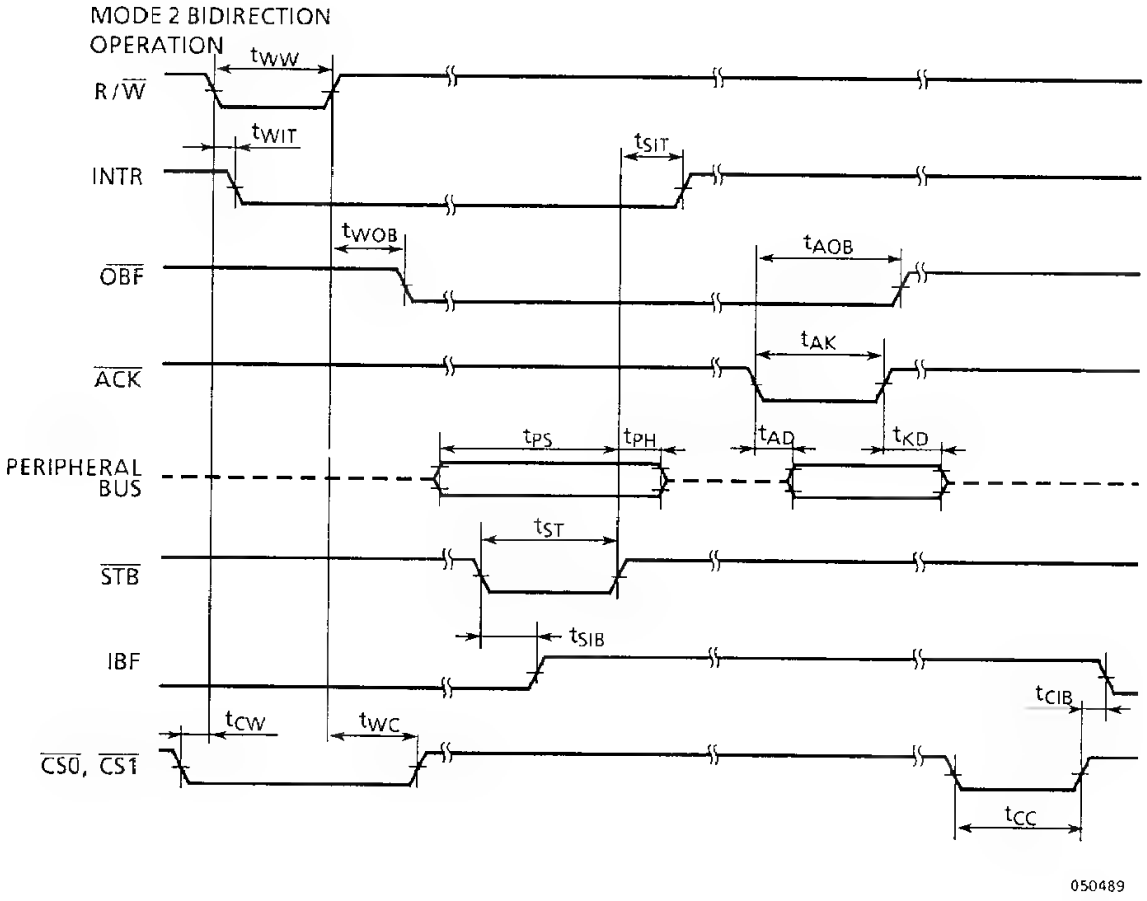


Figure 8.1 TMP82C255A Timing diagram (3)

8.2 TMP82C265A TIMING DIAGRAM (1)

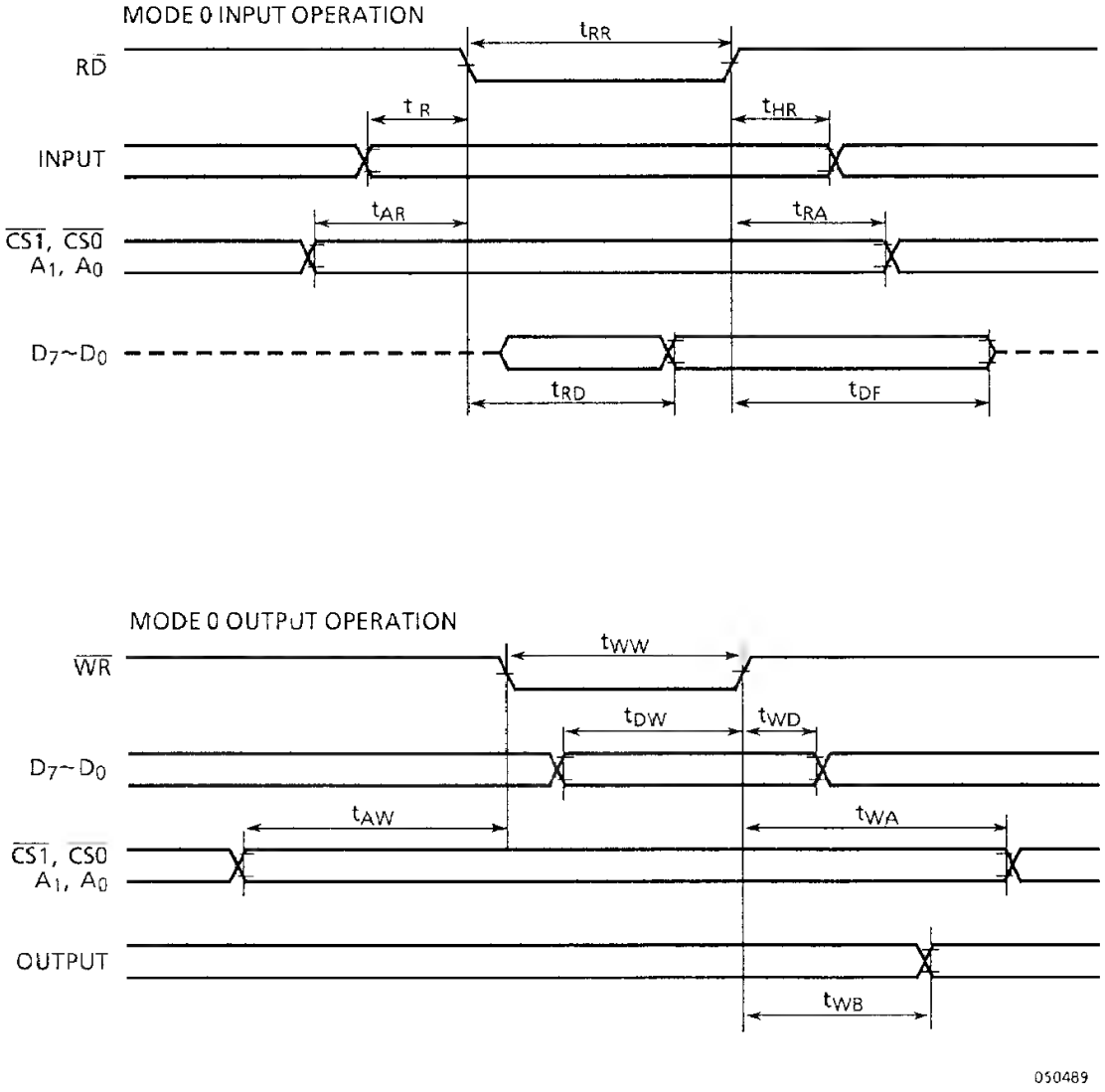


Figure 8.2 TMP82C265A Timing diagram (1)

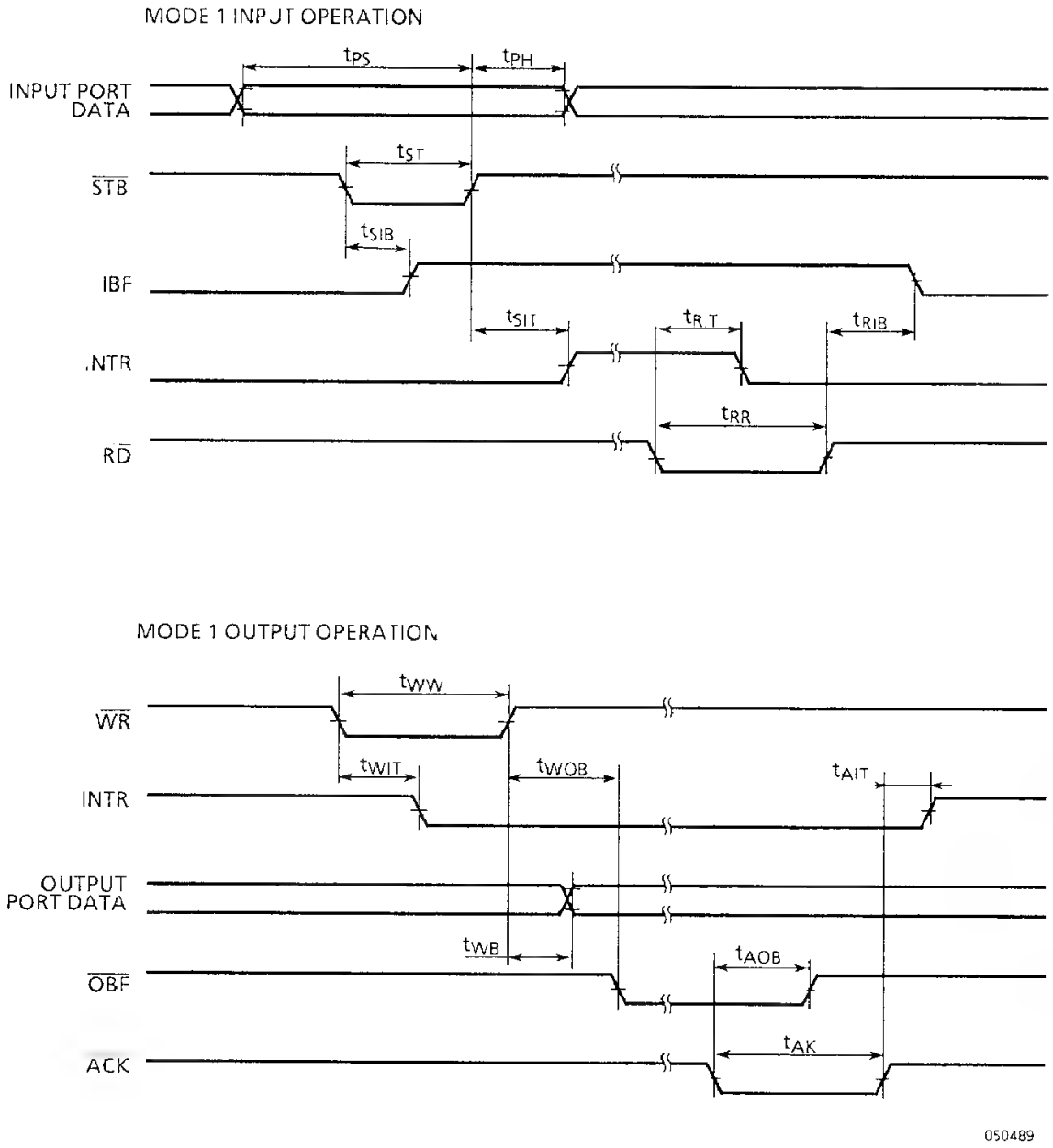


Figure 8.2 TMP82C265A Timing diagram (2)

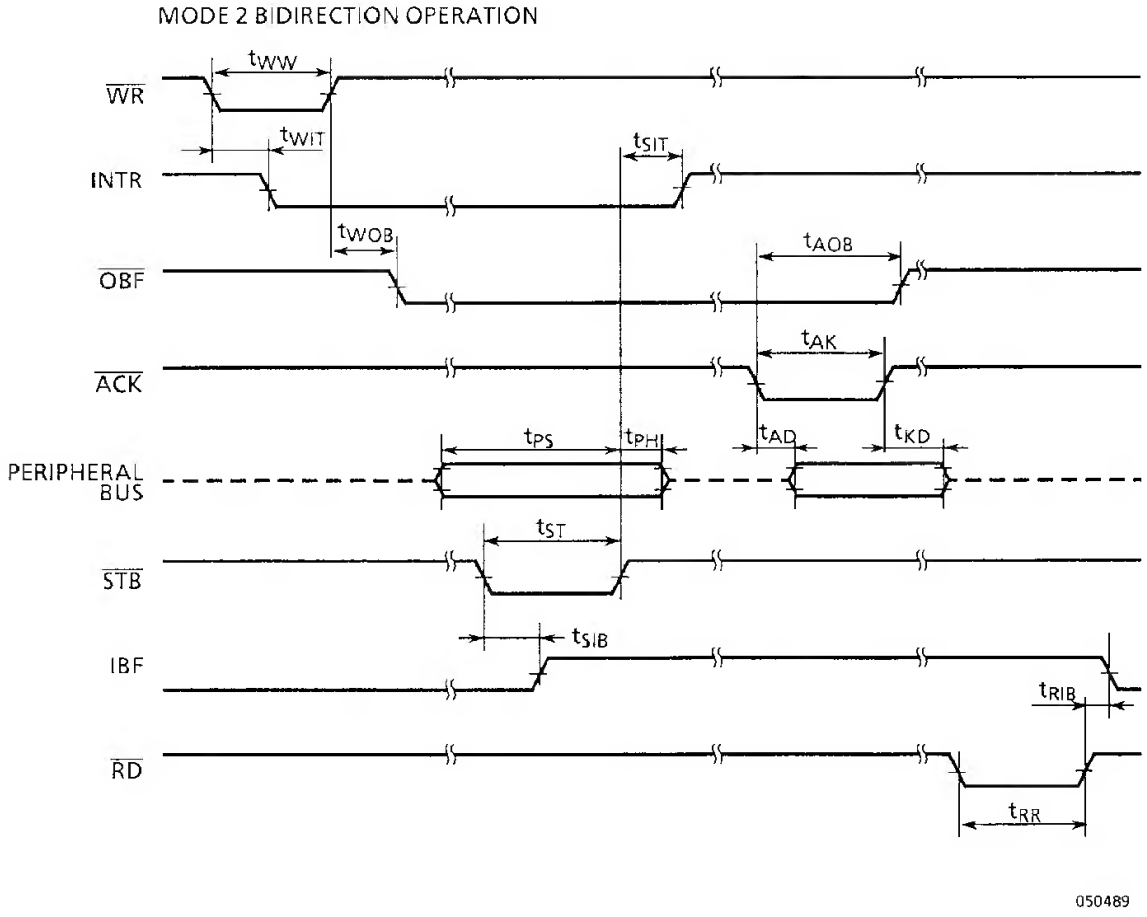
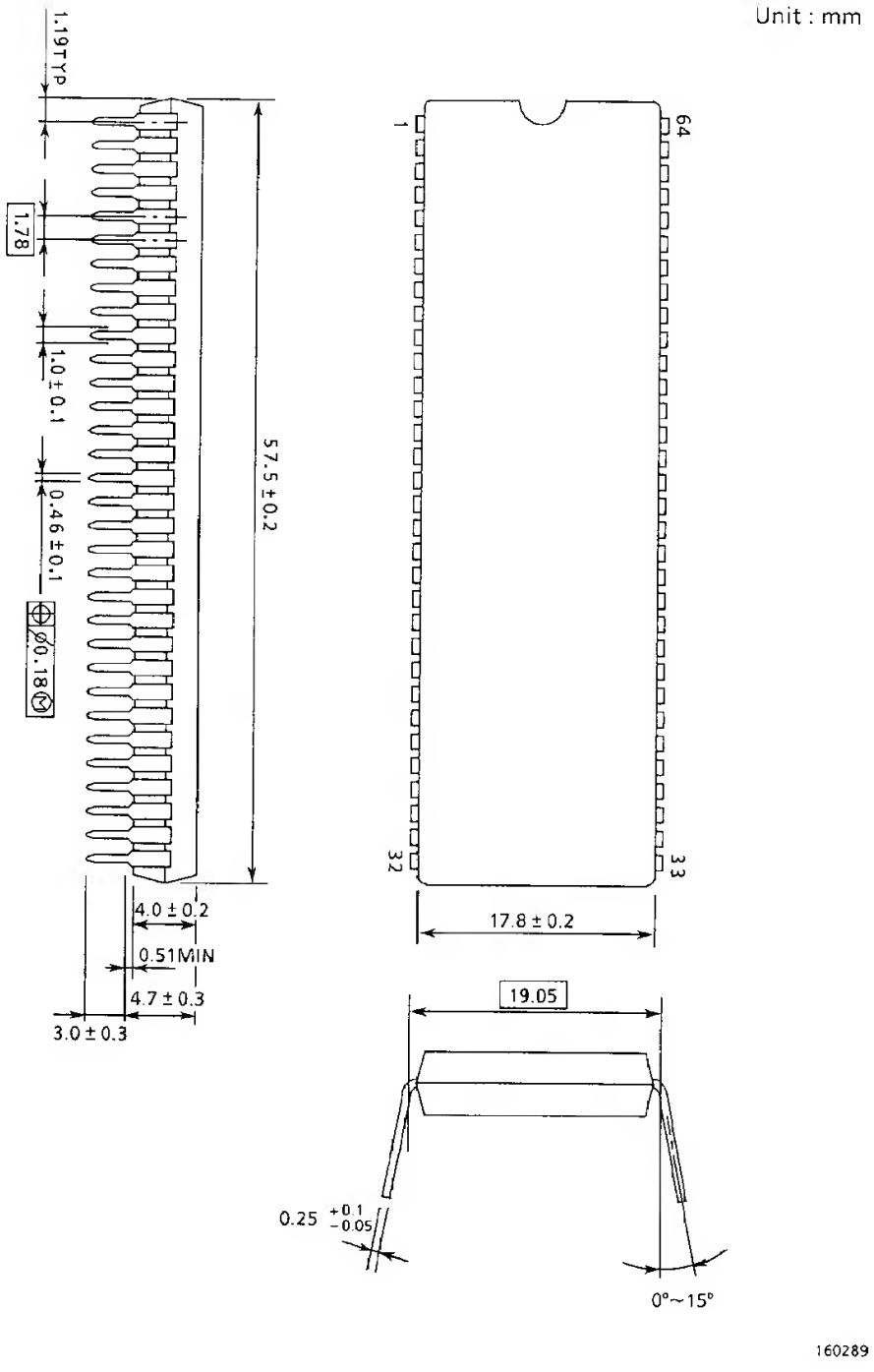


Figure 8.2 TMP82C265A Timing diagram (3)

9. OUTLINE DRAWINGS

SDIP64-P-750

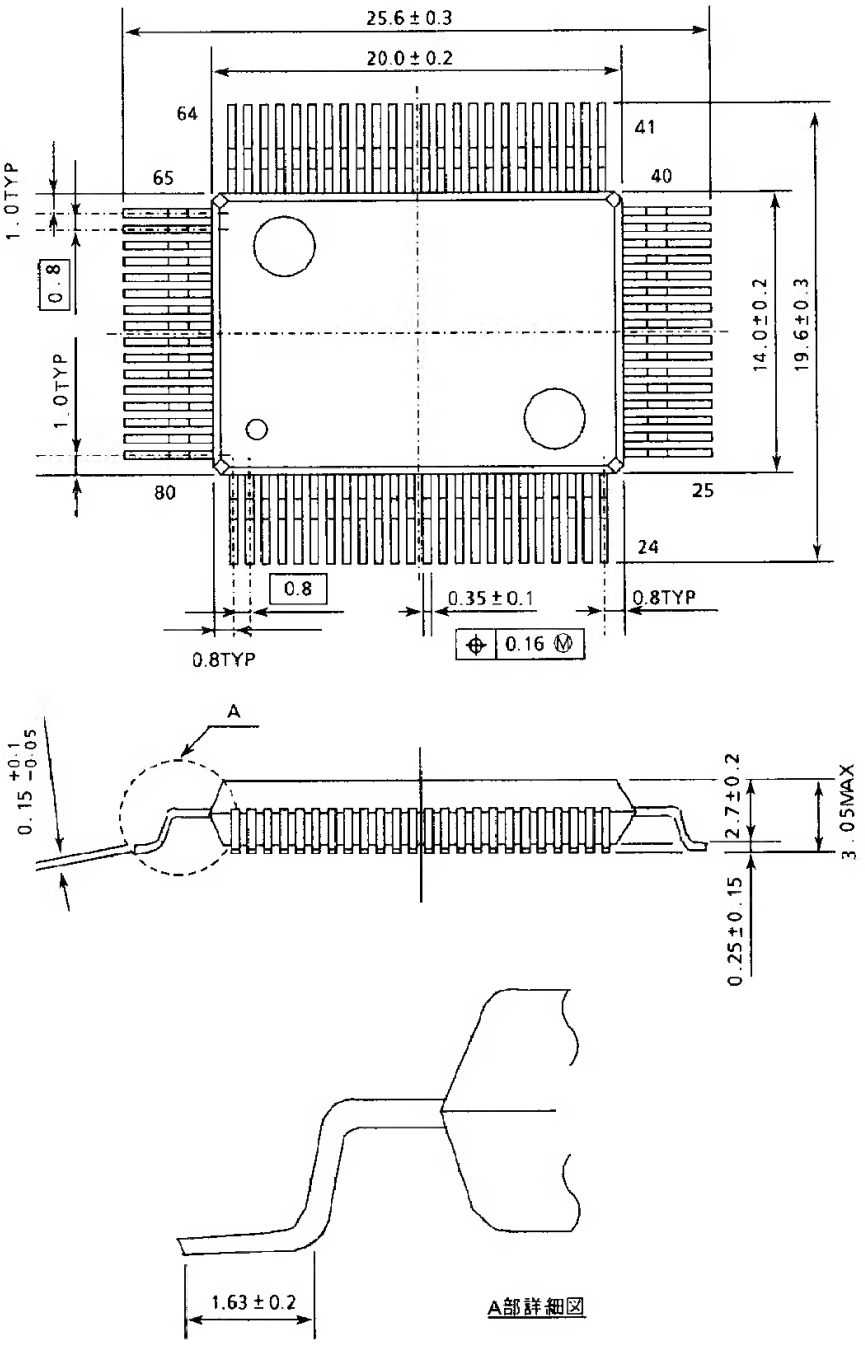
Unit : mm



Note : Each lead pitch is 1.78mm. All leads are located within 0.25mm of their trve longitudical position with respect to No.1 and No.64 leads.

QFP80-P-1420

Unit : mm



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